OIPE JC14
MAY 03 2004
PATENT & TRADEMARK OFFICE

#10
5-6-04

DECLARATION

I, Masayuki SAKAI, c/o Fukami Patent Office, of Mitsui Sumitomo Bank Minamimorimachi Building, 1-29, Minamimorimachi 2-chome, Kita-ku, Osaka-shi, Osaka, Japan, declare:

that I know well both the Japanese and English languages;

that to the best of my knowledge and belief the English translation attached hereto is a true and correct translation of Japanese Patent Application No. 10-317997, filed on November 9,1998;

that all statements made of my own knowledge are true;

that all statements made on information and belief are believed to be true; and

that the statements are made with the knowledge that willful false statements and the like are punishable by fine or imprisonment, or both, under 18 USC 1001.

Dated: April 12, 2004

Masayuki Sakai

OIPE
MAY 0 3 2004
PATENT & TRADEMARK OFFICE

日 本 国 特 許 庁
PATENT OFFICE
JAPANESE GOVERNMENT

別紙添付の書類に記載されている事項は下記の出願書類に記載されてる事項と同一であることを証明する。
This is to certify that the annexed is a true copy of the following application as filed h this Office.

出願年月日 Date of Application:	１９９８年１１月　９日 November 9, 1998
願番号 plication Number:	平成１０年特許願第３１７９９７号 Pat. Appln. No. 10-317997
願人 licant (s):	ミノルタ株式会社 MINOLTA CO., LTD.

１９９９年　７月１５日
July 15, 1999

特許庁長官
Commissioner,
Patent Office
伊佐山建志
Takeshi Isayama

出証番号　出証特平１１－３０５０４５６
Shutsu-sho-No. Shutsu-sho-toku-hei 11-3050456

[Document Name]	Petition for Patent
[Reference Number]	1980864
[Filing Date]	November 9, 1998
[Destination]	To the Commissioner of the JPO
[International Class]	G06F 1/00
[Title of the Invention]	Image Processing System
[Number of Claims]	3
[Inventor]	
[Address]	C/O MINOLTA CO., LTD., Osaka Kokusai Building, 3-13, 2-Chome, Azuchi-Machi, Chuo-Ku, Osaka-Shi, Osaka, Japan
[Name]	Junji NISHIGAKI
[Applicant]	
[Identification Number]	000006079
[Address]	Osaka Kokusai Building, 3-13, 2-Chome, Azuchi-Machi, Chuo-Ku, Osaka-Shi, Osaka, Japan
[Name]	MINOLTA CO., LTD.
[Attorney]	
[Identification Number]	100064746
[Patent Attorney]	
[Name]	Hisao FUKAMI
[Appointed Attorney]	
[Identification Number]	100085132
[Patent Attorney]	

[Name] Toshio MORITA

[Appointed Attorney]

[Identification Number] 100096792

[Patent Attorney]

[Name] Hachiro MORISHITA

[Indication of Fee]

[Deposit Account Number] 008693

[Fee] 21000

[List of the Accompanying Documents]

[Document]	Specification	1
[Document]	Drawings	1
[Document]	Abstract	1

[Number of General Power of Attorney] 9716296

[Document Name] Specification

[Title of the Invention] Image Processing System

[Claims for Patent]

1. An image processing system comprising:

synchronous type processing means for carrying out a first image process on image data that is the subject of processing;

asynchronous type processing means for carrying out a second image process on image data of a predetermined region of said image data that is the subject of processing; and

synthesize means for synthesizing an output of said synchronous type processing means and an output of said asynchronous type processing means to form one image data.

2. The image processing system according to claim 1, wherein said synthesize means comprises

a memory in which an output of said synchronous type processing means is stored, and

replacement means for replacing a portion of an output of said synchronous type processing means stored in said memory with an output of said asynchronous type processing means.

3. The image processing system according to claim 2, further comprising control means for controlling replacement timing by said replacement means by detecting status of an output of said synchronous type processing means stored in said memory.

[Detailed Description of the Invention]

[Technical Field to Which the Invention Belongs]

The present invention relates to image processing systems, particularly to an image processing system including a synchronous type processing means and an asynchronous type processing means.

[Conventional Art]

A conventional image processing apparatus is known that reads out image data stored in a memory to carry out image processing on the read out image data. The image processing apparatus can be formed of a synchronous type or an asynchronous type circuit. A hardware circuit such as the ASIC (application specific integrated circuit) is exemplary of the synchronous type circuit. A circuit that carries out a process with software formed of a MPU (microprocessor) and the like is exemplary of the asynchronous type circuit.

[Problems to be Solved by the Invention]

The conventional image processing apparatus imposes problems set forth in the following.

In an image processing apparatus entirely formed of the synchronous type circuit, the processing speed is determined by the process of the heavy load. There was a problem that the process is slowed down even if it is not necessary to carry out a heavy load process. This is because a process corresponding to the time consumed for the heavy load process is required whatever image data is processed. For example, in a synchronous type circuit 900 shown in Fig. 11 including a line memory 901, a matrix processing unit 903 and a γ correction unit 905, data delay occurs since image data of N lines must always be stored in line memory 901. Also, since a complicated matrix operation process (for example, integration of floating point) is carried out, data (operational result) delay occurs.

When the entirety is implemented by the synchronous type circuit, the synchronous circuit per se becomes complex and lacks flexibility. When the resolution or the like of the image data is altered, the entire structure of the apparatus must be modified, resulting in increase in cost.

When the entirety of the image processing apparatus is implemented by the asynchronous type circuit, high speed processing is degraded.

In view of the foregoing, an object of the present invention is to provide an

image processing apparatus that allows high speed processing, and that prevents increase in the cost when the resolution or the like is altered.

[Means for Solving the Problems]

According to an aspect of the present invention, an image processing system includes a synchronous type processing means for carrying out a first image process on image data that is the subject of processing, an asynchronous type processing means for carrying out a second image process on image data of a predetermined region out of the image data that is the subject of processing, and a synthesize means for synthesizing the output of the synchronous type processing means with the output of the asynchronous type processing means to form one image data.

Preferably, the synthesize means includes a memory storing the output of the synchronous type processing means, and a replacement means for replacing a portion of the output of the synchronous type processing means stored in the memory with the output of the asynchronous type processing means.

Further preferably, the image processing system includes a controller controlling the replacement timing by the replacement means by detecting the state of the output of the synchronous type processing means stored in the memory.

The asynchronous type processing means carries out a second image process only on image data of a predetermined region. Therefore, an image processing system that allows high speed processing is provided. When there is no predetermined region on which the second image process is to be carried out, only the output of the synchronous type processing means is to be used. Therefore, high speed processing is allowed.

The asynchronous type processing means has flexibility. Therefore, it is easy to modify only the processing contents that require modification (for example N-dimensional process) when the resolution or the like of the image data is altered. Thus, increase in the cost can be suppressed even in the case where the resolution or the like is altered.

By carrying out the second image process through the asynchronous processing means during the process through the synchronous type processing means, the process can be further speeded.

[Embodiments of the Invention]

Fig. 1 is a diagram to describe an operation of an image processing apparatus according to an embodiment of the present invention. Referring to Fig. 1, an image process of light load is carried out on the entire region of document image data 100 by means of a synchronous type circuit. The result is written into a memory. An asynchronous circuit carries out a process such as matrix operation on regions (for example, text region) 100a and 100b in document image data 100 that require processing of heavy load. The processed result of the asynchronous type circuit is overwritten on the memory in which the processed result of the synchronous type circuit has been written.

The synchronous type circuit carries out high speed image processing on the entire region of the document image data whereas the asynchronous type circuit carries out image processing exclusively on the region that requires heavy load processing such as a matrix operation. The process carried out by the synchronous type circuit includes the one-dimensional process such as γ correction. The process carried out by the asynchronous circuit includes the two-dimensional process such as edge enhancement process on a text region and smoothing process on a halftone dot region.

By virtue of the flexibility of the asynchronous type circuit, the processing contents can be modified easily when the resolution or the like of the image data is altered. Therefore, increase in cost can be suppressed.

Fig. 2 is a diagram to describe in further detail the operation of the image processing apparatus. Referring to Fig. 2, the image of interest is stored in an input image memory having the capacity of WX pixels horizontally and WY pixels vertically. Data IDi of one pixel in the input image memory is read out in series and subjected to γ correction with a predetermined function to become γ corrected data ODi1.

γ corrected data ODi1 is recorded at a corresponding address in the output image memory. γ correction is carried out on all the pixels.

Then, a matrix operation is carried out on a pixel in a predetermined region in the input image memory. It is assumed that the address of the pixel that is the subject of matrix operation is (i, j), and data of that address is D (i, j). The matrix has the size of M laterally and N vertically. Data subjected to the matrix operation is represented by the following equation (1).

$$T \Sigma k(i, j) \cdot D(i, j) \qquad (1)$$

where T, k (i, j) are constants, and i = 0 - (M - 1), j = 0 - (N - 1). Then, γ correction is carried out on this data to result in data ODi2.

First, γ corrected data ODi1 is written into the output image memory, and then data ODi2 is written into a predetermined region.

[First Embodiment]

Fig. 3 is a block diagram showing a structure of an image processing apparatus according to a first embodiment of the present invention. Referring to Fig. 3, the image processing apparatus includes an input image memory 201, an input memory control unit 203, a γ correction unit 205, an output memory control unit 207, a matrix operation unit 209, and an output image memory 211. For the process of input data, a data bus for input data is used. For the process of the output data, a data bus for output data is used.

Image data input by means of a scanner and the like is stored in input image memory 201. The storage capacity of input image memory 201 corresponds to WX × WY for a monochromatic image, corresponds to WX × WY × 3 for a color (RGB) image, and corresponds to WX × WY × 4 for a color (CMYK) image, when the size of the image data is (number of main scanning pixels, number of sub scanning pixels) = (WX, WY). For the sake of simplification, it is assumed that the storage capacity of input image memory 201 is WX × WY in the following. Although image data coding is not effected in the present embodiment, the memory capacity of input image memory

201 can be reduced by carrying out a coding process.

Input memory control unit 203, γ correction unit 205 and output memory control unit 207 are implemented by an ASIC circuit that allows high speed processing since the circuits are formed of relatively simple logics. Matrix operation unit 209 is formed of a MPU (microprocessor) that allows complicated operation to read out image data of M × N pixels and apply a complicated operation thereon.

Under DMA (direct memory access) control, input memory control unit 203 reads out image data stored in input image memory 201 sequentially from the start address to the end address (start address + WX × WY). Input memory control unit 203 includes an internal register in which a status flag (imb flag) is held indicating whether access to input image memory 201 is busy or not.

γ correction unit 205 converts and outputs the input data according to a table of output data (8 bits: 0 - 255) corresponding to the input data (8 bits: 0 - 255).

Under DMA control, output memory control unit 207 sequentially writes the γ-corrected data from the start address up to the end address (start address + WX × WY) into output image memory 211. Output memory control unit 207 includes an internal register in which a status flag (omb flag) is held indicating whether access to output image memory 211 is busy or not.

Matrix operation unit 209 monitors the imb flag of input memory control unit 203 to read out the data of M × N pixels including the target pixel by random access from input image memory 201 when the imb flag indicates a non-busy state. Then, the matrix operation such as edge enhancement is carried out on the text region and smoothing on the halftone region. Matrix operation unit 206 further carries out a process likewise the γ correction formed of logic. Matrix operation unit 209 monitors the omb flag of output memory control unit 207 to write the resultant data of the matrix operation into the address of output image memory 211 corresponding to the target pixel when the omb flag indicates a non-busy state. Accordingly, γ-corrected data from γ correction unit 205 is replaced in output image memory 211.

The region on which matrix operation is to be carried out can be determined by matrix operation unit 209. Alternatively, a region determined in advance can be input through the data bus.

The output image data subjected to γ correction and matrix operation in output image memory 211 is provided to a printer engine and the like through the data bus.

When image data is written into input image memory 201 in the present embodiment, input memory control unit 203, γ correction unit 205 and output memory control unit 207 carry out a one-dimensional process of light load such as γ correction on the image data in input image memory 201. Since the imb flag in input memory control unit 203 indicates a busy state during this process, matrix operation unit 209 cannot read out data from input image memory 201.

Following the γ correction on all the image data in input image memory 201, matrix operation unit 209 extracts image data that is the subject of processing from a predetermined region of the image data stored in input image memory 201. A two-dimensional process is applied on the extracted image data. The processed result is overwritten on the predetermined region in output image memory 211.

Fig. 4 is a flow chart for describing the process carried out by matrix operation unit 209. Referring to Fig. 4, initialization is carried out at step S101. At S103, the address of the target pixel that becomes the subject of processing in input image memory 201 is determined. At step S105, the access status (imb flag) of input memory control unit 203 is confirmed. Waiting is conducted when the imb flag indicates a busy state (S107).

When the imb flag indicates a non-busy state, control proceeds to step S109 where image data of the matrix of M × N centered about the target pixel is read out. At step S111, the operation process of the M × N matrix is carried out.

At step S113, γ correction is carried out on the image data subjected to the operation process.

At step S115, the access state (omb flag) of output memory control unit 207 is

confirmed. At step S117, waiting is conducted until the omb flag of output memory control unit 207 indicates a non-busy state. At step S119, the write address of output image memory 211 is confirmed by output memory control unit 207. This causes the writing of the data subjected to matrix operation to attain a standby state until γ-corrected data is written into the address of the target pixel by output memory control unit 207. At step S121, the data subjected to matrix operation is overwritten in output image memory 211.

At step S123, determination is made whether all matrix operation has been completed. The routine ends when YES. When NO at step S123, control returns to step S103.

According to the above-described steps of S105 and 107, matrix operation unit 209 reads out the image data from input image memory 201 when input memory control unit 203 is not busy. Accordingly, the access of input image memory 201 by input memory control unit 203 is given priority.

By the above-described steps of S115 and S117, the writing operation by matrix operation unit 209 is carried out when output memory control unit 207 is not busy. Accordingly, access to output image memory 211 by output memory control unit 207 is given priority. A memory storing the processed result of one line can be provided in output memory control unit 207. Output memory control unit 207 may access output image memory 211 only when the process of one line has been completed by output memory control unit 207 and the process of the next line has not yet been initiated.

[Second Embodiment]

The image processing apparatus according to the second embodiment of the present invention has a structure identical to that of the first embodiment. Therefore, description thereof will not be repeated. The image processing apparatus of the second embodiment executes the flow chart represented in Fig. 5 instead of the process represented in Fig. 4. The image processing apparatus of the present embodiment is characterized in that a halftone region or an edge region is detected and image

processing carried out on the detected region by scanning the image data stored in input image memory 201.

Referring to Fig. 5, initialization is carried out at step S201. At step S203, determination is made whether input image memory 201 can be accessed or not by referring to the imb flag. Waiting is conducted until access is allowed.

At step S205, a matrix of 5 × 5 pixels centered about the target pixel is extracted from the image data stored in input image memory 201. At step S207, determination is made whether the target pixel is an isolated point or not. When YES at S207, control proceeds to step S209 where a larger matrix of 9 × 41 pixels is extracted, and then determination is made whether that matrix corresponds to a halftone image or not (S211).

When YES at S211, control proceeds to step S213 to carry out a smoothing process using the data of the 5 × 5 pixels. Then, control proceeds to step S215 to carry out a γ correction. At step S217, the omb flag is confirmed to determine whether access to output image memory 211 is allowed or not. When access to output image memory 211 is allowed, control proceeds to step S219 to write the data into output image memory. At step S221, determination is made whether the process has been completed for all the data. When YES at step S221, the routine ends.

When NO at step S221, control returns to step S203. Also, when NO at step S221, control proceeds to step S221.

When determination is made that the target pixel is not an isolated point at step S207, control proceeds to step S223 to determine whether the subject is an edge image. When YES, control proceeds to step S225 to carry out edge enhancement. Then, control proceeds to step S215.

When NO at step S223, control proceeds to step S221.

The processing time by the matrix operation unit according to the present embodiment is set forth in the following.

(processing time of target pixel when corresponding to halftone dot) = (matrix

read out time of 5 × 5 pixels) + (time for determining an isolated point) + (matrix read out time of 9 × 41 pixels) + (time for determining halftone dot) + (time for smoothing process of 5 × 5 pixels) + (time for γ correction)

(processing time of target pixel when corresponding to edge) = (matrix read out time of 5 × 5 pixels) + (time for determining an isolated point) + (time for edge enhancement process of 5 × 5 pixels) + (time for γ correction)

(processing time of target pixel when not corresponding to edge or halftone dot, and is not an isolated point) = (matrix read out time of 5 × 5 pixels) + (time for determining an isolated point)

(processing time of target pixel when not corresponding to edge or halftone dot, and is an isolated point) = (matrix read out time of 5 × 5 pixels) + (time for determining an isolated point) + (matrix read out time of 9 × 41 pixels) + (time for determining a halftone dot)

In view of the foregoing, the relationship of the processing time is established as follows:

(processing time of target pixel when not corresponding to edge or halftone dot, and is not an isolated point) < (processing time of target pixel when corresponding to edge) < (processing time of target pixel when not corresponding to edge or halftone dot, and is an isolated point) < (processing time of target pixel corresponding to halftone dot).

[Third Embodiment]

Fig. 6 is a block diagram showing a structure of an image processing apparatus according to a third embodiment of the present invention. The image processing apparatus of the third embodiment corresponds to the image processing apparatus of the

first embodiment shown in Fig. 3 with a region determination memory 251 connected to the data bus. Determination of a region of the image data stored in input image memory 201 is recorded in advance in region determination memory 251. In the present embodiment, region determination memory 251 distinguishes whether one pixel of the image data stored in input image memory 201 corresponds to an edge region, a halftone region, or a region other than the edge or halftone region.

Fig. 7 is a flow chart of the process carried out by matrix operation unit 209 of the third embodiment. Referring to the Fig. 7, at step S301, initialization is carried out. At step S303, the address of the target pixel is extracted.

At step S305, determination is made whether the target pixel corresponds to an edge region or a halftone region by region determination memory 251. When the target pixel corresponds to an edge or halftone region, control proceeds to step S307 to determine whether access to input image memory 201 is allowed or not through the imb flag. Waiting is conducted until access is allowed. At step S309, the data of the matrix of 5×5 pixels around the target pixel is read out. A smoothing process is carried out if the target pixel corresponds to a halftone region (S311). An edge enhancement process is carried out if the target pixel corresponds to an edge region (S321). Then, γ correction is carried out on the data of the target pixel (S313). Next, determination is made whether output image memory 211 can be accessed or not through the omb flag. Waiting is conducted until access is allowed (S315).

At step S317, image data is written into output image memory 211. At step S319, determination is made whether the process of all the data has been completed or not. When YES at step S319, the main routine ends.

When NO at step S319, control returns to step S303. When NO at S305, control proceeds to step 319.

The processing time by the matrix operation unit in the third embodiment is set forth in the following.

(processing time of target of interest when corresponding to a halftone dot) =

(time for reading out determination result of target pixel) + (read out time of 5 × 5 pixels) + (time for smoothing process of 5 × 5 pixels) + (time for γ correction)

(processing time of target pixel when corresponding to edge) = (time for reading out determination result of target pixel) + (read out time of 5 × 5 pixels) + (processing time for edge enhancement of 5 × 5 pixels) + (time for γ correction)

(processing time of target pixel when not corresponding to edge or halftone dot) = (time for reading out determination result of target pixel)

In view of the foregoing, the relationship of the processing time is established as follows:

(processing time of target pixel when not corresponding to edge or halftone dot) < (processing time of target pixel when corresponding to halftone dot) < (processing time of target pixel when corresponding to edge)

[Fourth Embodiment]

Fig. 8 is a block diagram showing a structure of an image processing apparatus according to a fourth embodiment of the present invention. The image processing apparatus of the present embodiment differs from the image processing apparatus of Fig. 3 in that input image memory 301 and output image memory 311 are set as dual port memories. Accordingly, the process by the synchronous type circuit and the process by the asynchronous type circuit can be carried out in parallel to further increase the image processing speed.

Fig. 9 is a flow chart of the process carried out by a matrix operation unit 309 according to the image processing apparatus of the fourth embodiment. The flow chart of Fig. 9 differs from the flow chart of Fig. 4 in that the step of identifying the access status of the input image memory and the output image memory through the imb flag

and the omb flag (steps S105, S107, S115 and S117 of Fig. 4) is deleted. This is because matrix operation unit 309 can access the memory any time without taking account of the access to the memory in the fourth embodiment.

It is to be noted that the output result of matrix operation unit 309 must be overwritten after the output result of the synchronous type circuit is written into output image memory 311. Therefore, control is provided so that the writing status into output image memory 311 by output memory control unit 307 is identified at step S419 of Fig. 9 to allow the operation result of matrix operation unit 309 to be written into output image memory 311 after the output result from the synchronous type circuit is written.

[Effects of the image processing system of the above-described embodiments]

Fig. 10 is a diagram to describe the advantage of the image processing apparatus of the present invention. It is assumed that the relative ratio of the image processing time is γ correction (one-dimensional process): text correction (5×5 matrix operation) = 1 : 25 and one page of image data is formed of 100 pixels. When the entire process is carried out by a synchronous type circuit, the processing time of one page is 100 (pixels) $\times$ 25. When only the γ correction is carried out by the synchronous type circuit as in the above embodiments, the processing time is 50 (pixels) $\times$ 25 and 25 (pixels) $\times$ 25 in the case where the text is distributed for 50% and 25% in one page, respectively.

In other words, the processing time becomes longer when the all the process is carried out by a synchronous type circuit since text correction (5×5 matrix operation) is carried out on all the pixels irrespective of the text distribution. In contrast, only the required portion is subjected to text correction by virtue of the usage of both a synchronous type circuit and an asynchronous type circuit as in the above embodiments. Therefore, the processing speed is improved.

In the above embodiments, the processes are executed within a unitary apparatus. However, the processes can be carried out by a plurality of apparatuses. For example, the synchronous processing unit and the asynchronous processing unit can be

implemented by separate apparatuses.

A program for executing the above process (S101 - S123) stored in a storage medium can be loaded into the matrix operation unit and executed therewith.

Although the present invention has been described and illustrated in detail, it is clearly understood that the same is by way of illustration and example only and is not to be taken by way of limitation, the spirit and scope of the present invention being limited only by the terms of the appended claims.

[Brief Description of the Drawings]

Fig. 1 is a diagram to describe an operation of an image processing apparatus according to the present invention.

Fig. 2 is a diagram to describe in further detail the process of Fig. 1.

Fig. 3 is a block diagram of an image processing apparatus according to a first embodiment of the present invention.

Fig. 4 is a flow chart of the process of a matrix operation unit 209 of Fig. 3.

Fig. 5 is a flow chart of the process carried out by the matrix operation unit of an image processing apparatus according to a second embodiment of the present invention.

Fig. 6 is a block diagram of an image processing apparatus according to a third embodiment of the present invention.

Fig. 7 is a flow chart of a process of a matrix operation unit 209 of Fig. 6.

Fig. 8 is a block diagram showing the structure of an image processing apparatus according to a fourth embodiment of the present invention.

Fig. 9 is a flow chart of a process of a matrix operation unit 309 of Fig. 8.

Fig. 10 is a diagram to describe the advantage of the image processing apparatus of the present invention.

Fig. 11 is a block diagram showing an example of an image processing apparatus formed of only a synchronous circuit.

[Description of the Reference Characters]

201, 301 input image memory

203, 303 input image control unit

205, 305 γ correction unit

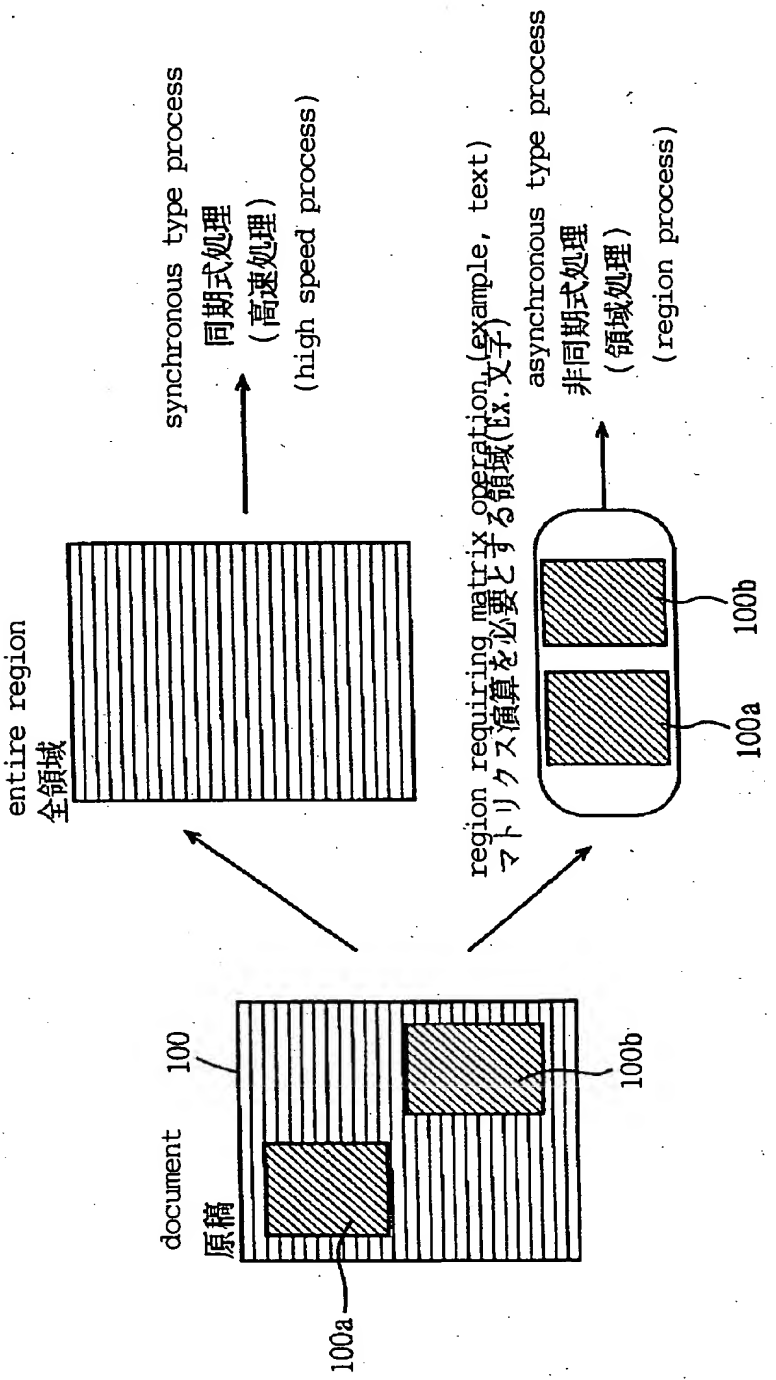
209, 309 matrix operation unit

211, 311 output image memory

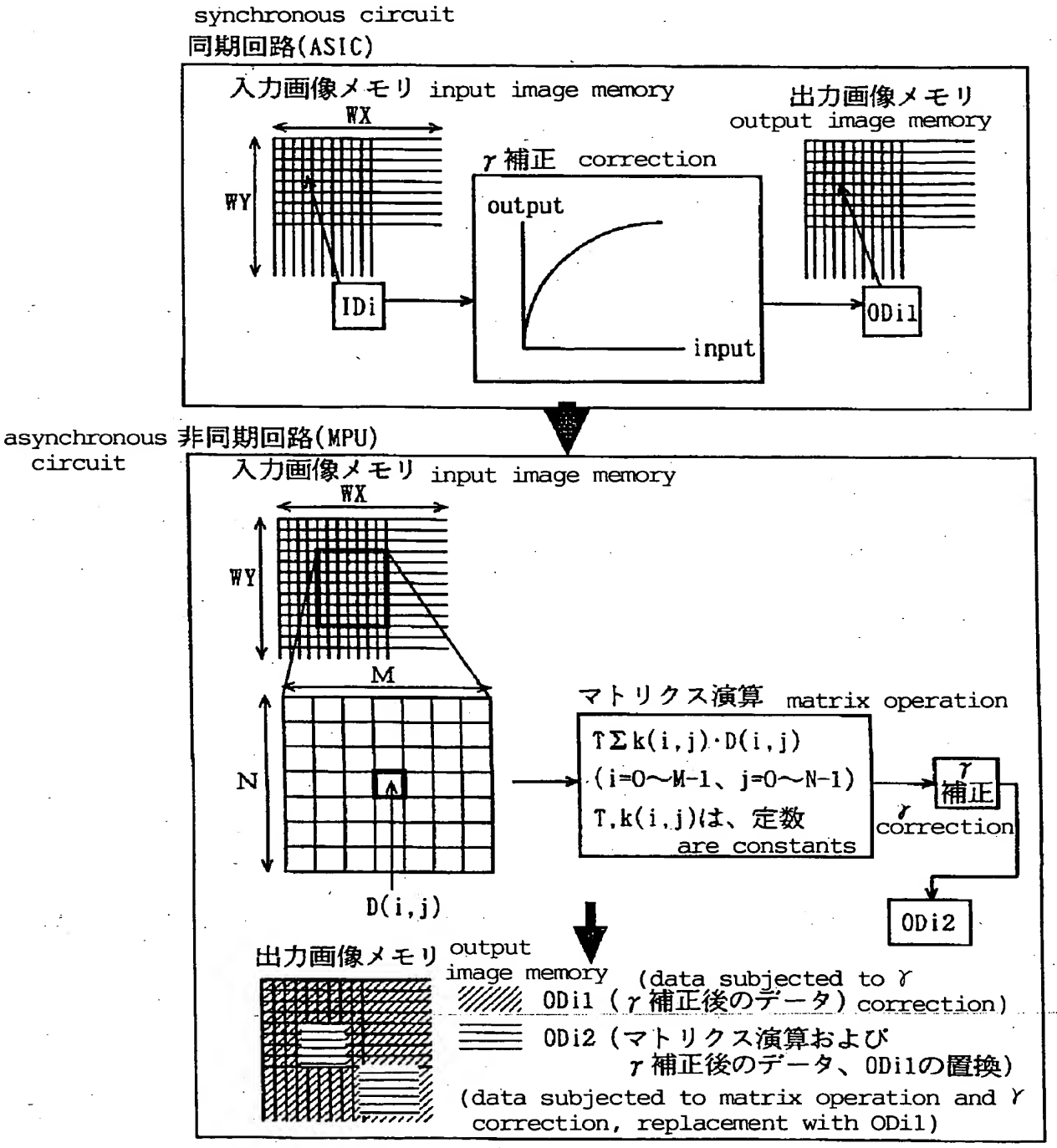
251 region determination memory

【書類名】　図面　document name　drawings

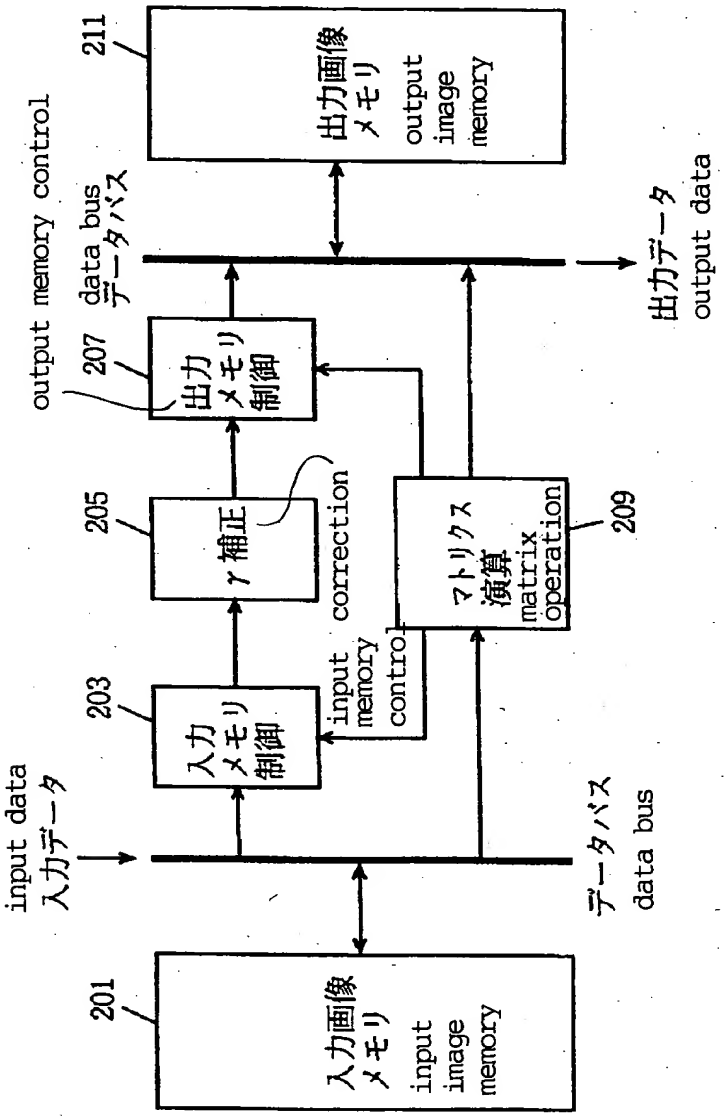
【図１】
Fig. 1



【図２】
Fig. 2

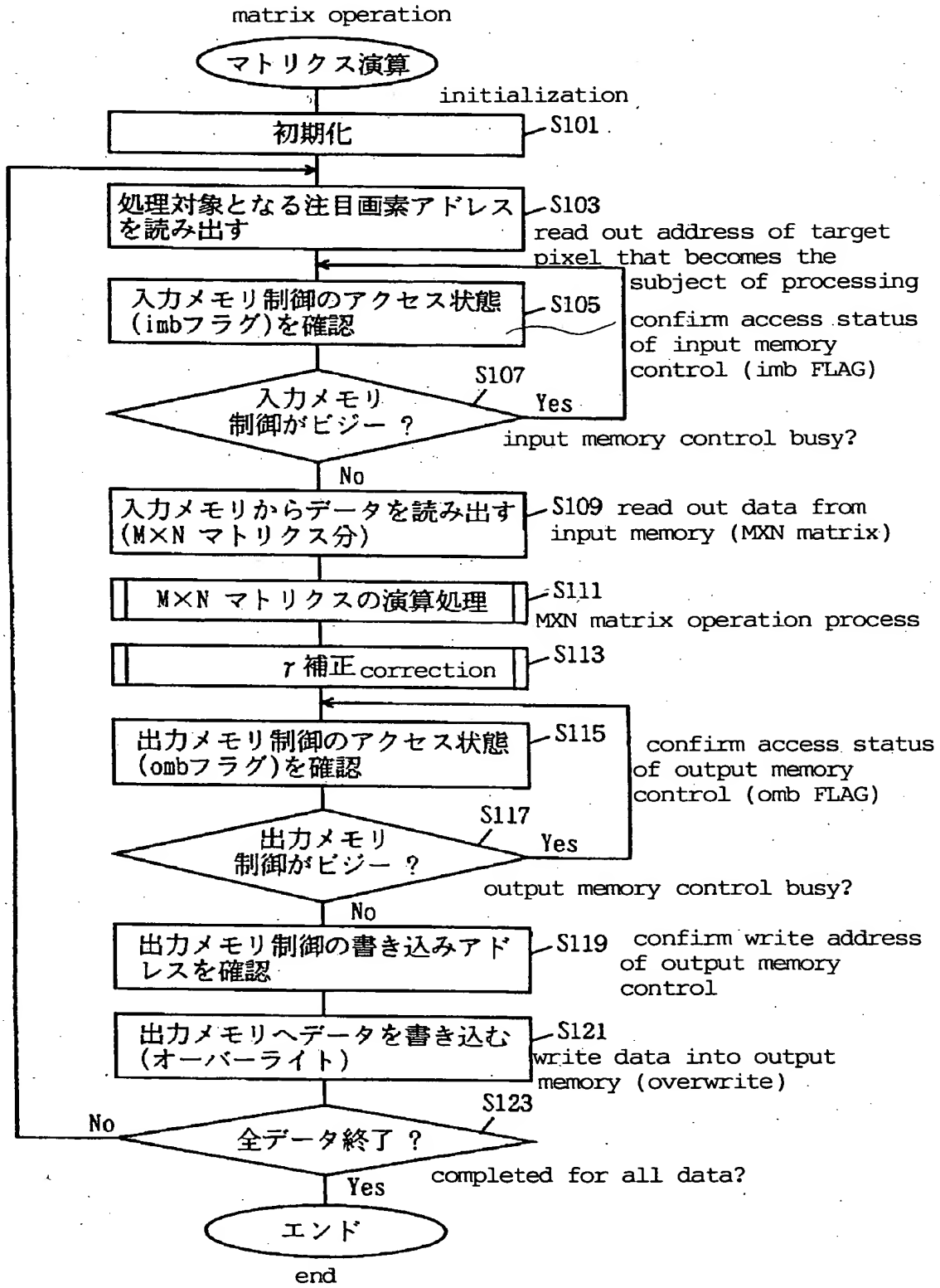

synchronous circuit
同期回路(ASIC)
入力画像メモリ input image memory
WX
WY
IDi
γ補正 correction
output
input
出力画像メモリ
output image memory
ODi1
asynchronous circuit
非同期回路(MPU)
入力画像メモリ input image memory
WX
WY
M
N
D(i,j)
マトリクス演算 matrix operation
T Σ k(i,j)·D(i,j)
(i=0～M-1、j=0～N-1)
T,k(i,j)は、定数
are constants
γ補正
γ correction
ODi2
出力画像メモリ
output image memory
ODi1 (γ補正後のデータ) (data subjected to γ correction)
ODi2 (マトリクス演算および γ補正後のデータ、ODi1の置換)
(data subjected to matrix operation and γ correction, replacement with ODi1)

【図３】
Fig. 3

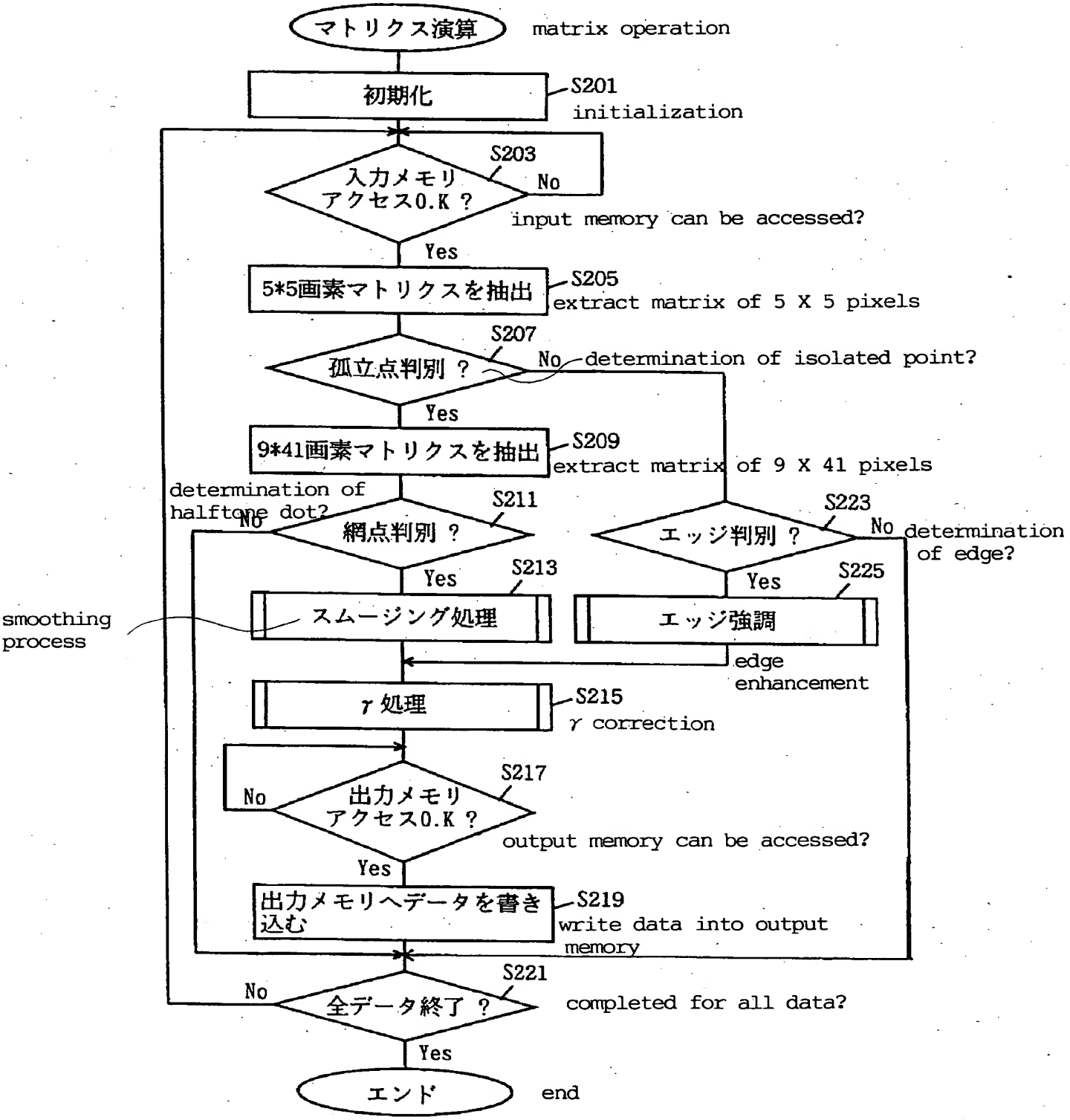

211
出力画像メモリ
output image memory
output memory control
data bus データバス
出力データ
output data
207
出力メモリ制御
205
γ補正
correction
マトリクス演算
matrix operation
209
input memory control
203
入力メモリ制御
input data
入力データ
データバス
data bus
201
入力画像メモリ
input image memory

【図４】

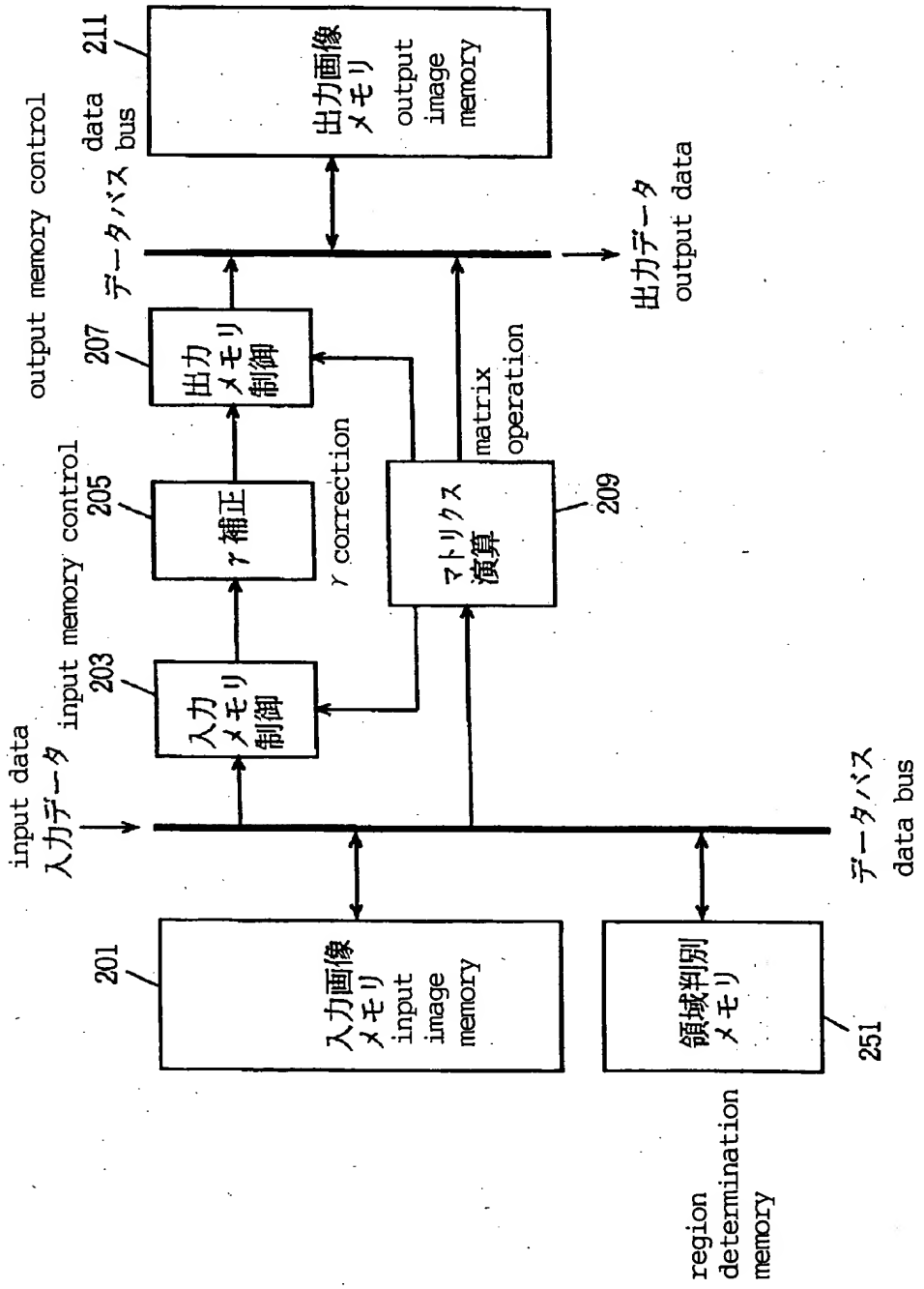
Fig. 4


matrix operation
マトリクス演算
initialization
初期化
S101
処理対象となる注目画素アドレスを読み出す
S103
read out address of target pixel that becomes the subject of processing
入力メモリ制御のアクセス状態(imbフラグ)を確認
S105
confirm access status of input memory control (imb FLAG)
S107
入力メモリ制御がビジー ?
Yes
input memory control busy?
No
入力メモリからデータを読み出す(M×N マトリクス分)
S109 read out data from input memory (MXN matrix)
M×N マトリクスの演算処理
S111
MXN matrix operation process
γ補正 correction
S113
出力メモリ制御のアクセス状態(ombフラグ)を確認
S115
confirm access status of output memory control (omb FLAG)
S117
出力メモリ制御がビジー ?
Yes
output memory control busy?
No
出力メモリ制御の書き込みアドレスを確認
S119
confirm write address of output memory control
出力メモリへデータを書き込む(オーバーライト)
S121
write data into output memory (overwrite)
S123
No
全データ終了 ?
completed for all data?
Yes
エンド
end

【図５】
Fig. 5

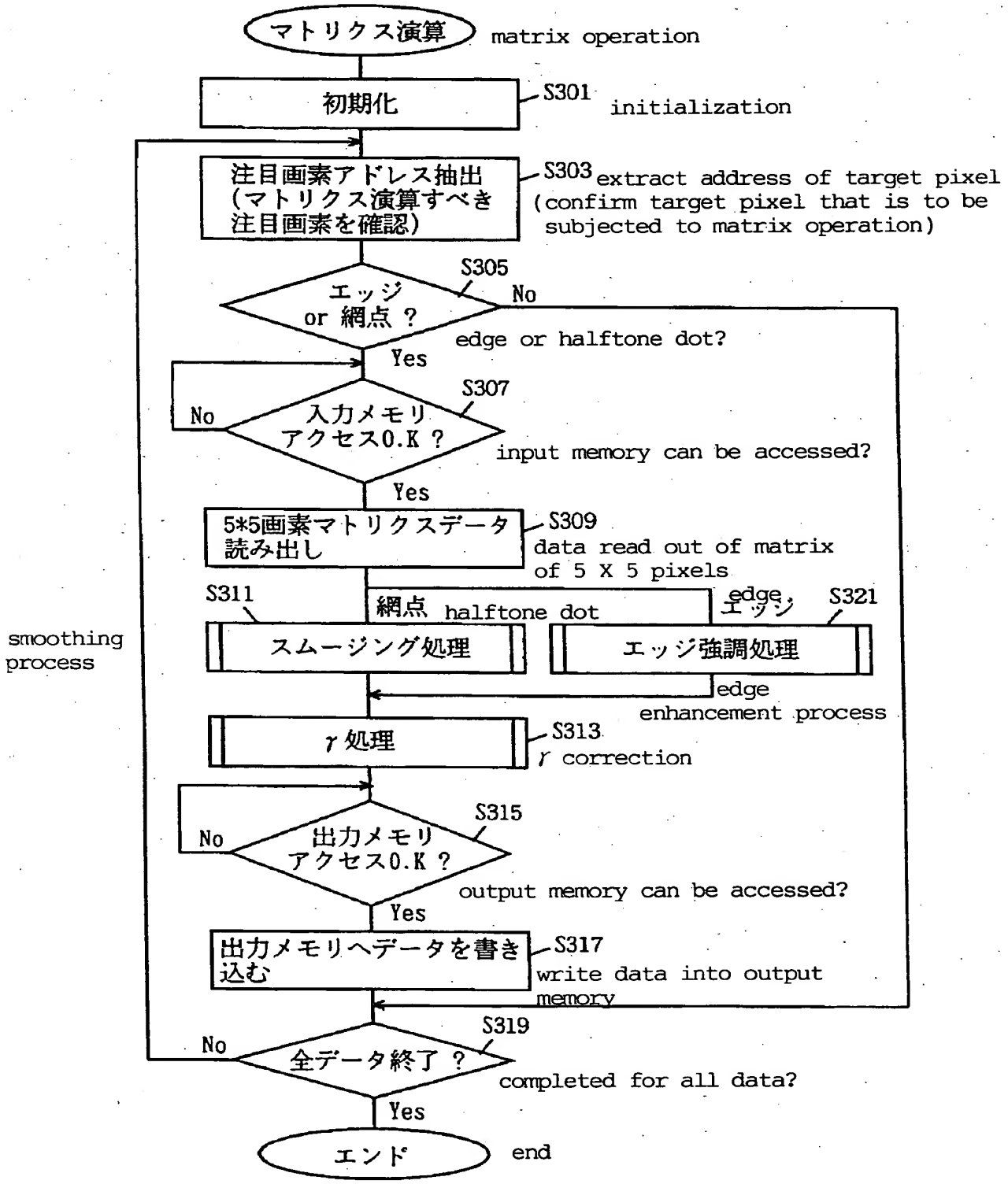

マトリクス演算
matrix operation
初期化
S201
initialization
S203
入力メモリ
アクセスO.K ?
No
input memory can be accessed?
Yes
5*5画素マトリクスを抽出
S205
extract matrix of 5 X 5 pixels
S207
孤立点判別 ?
No
determination of isolated point?
Yes
9*41画素マトリクスを抽出
S209
extract matrix of 9 X 41 pixels
determination of halftone dot?
S211
網点判別 ?
No
Yes
S213
スムージング処理
smoothing process
S223
エッジ判別 ?
No
determination of edge?
Yes
S225
エッジ強調
edge enhancement
γ処理
S215
γ correction
S217
No
出力メモリ
アクセスO.K ?
output memory can be accessed?
Yes
出力メモリへデータを書き込む
S219
write data into output memory
S221
No
全データ終了 ?
completed for all data?
Yes
エンド
end

【図６】
Fig. 6

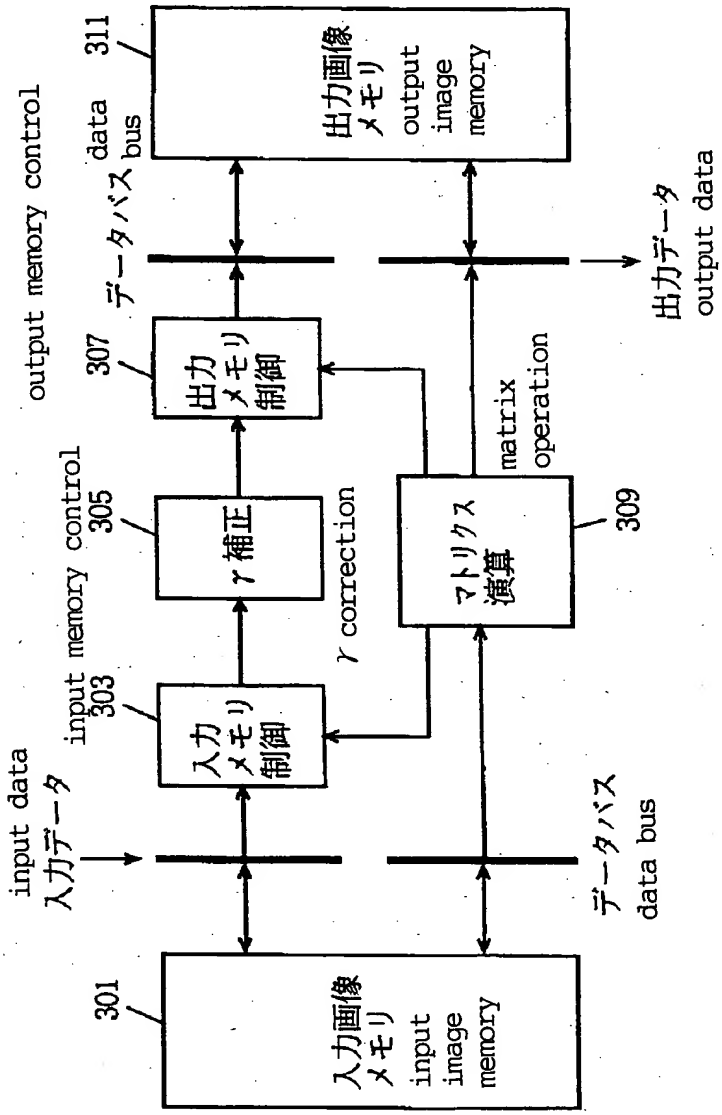

入力画像メモリ
input image memory
201
領域判別メモリ
251
region determination memory
データバス
data bus
input data
入力データ
入力メモリ制御
input memory control
203
γ補正
205
γ correction
マトリクス演算
209
matrix operation
出力メモリ制御
207
output memory control
出力画像メモリ
output image memory
211
出力データ
output data

【図７】

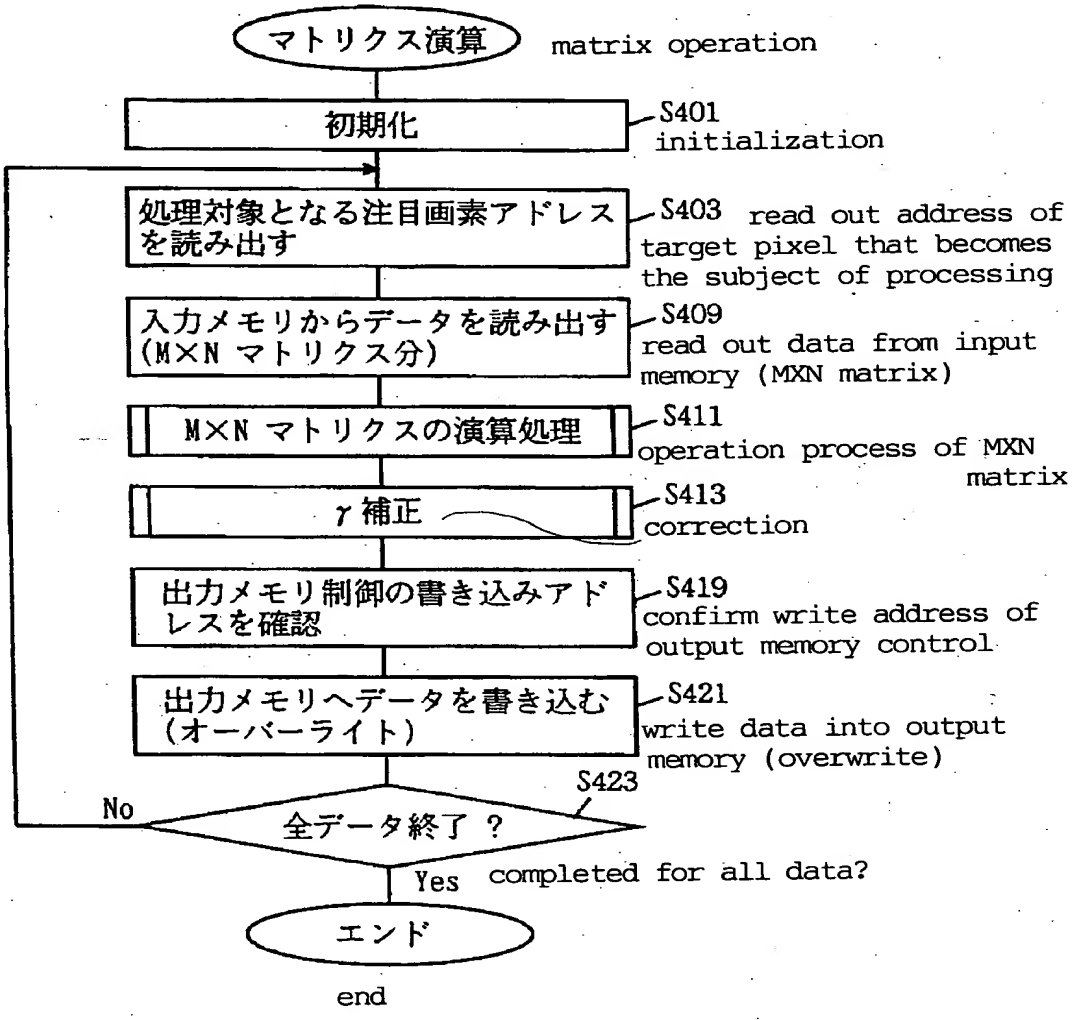
Fig. 7


マトリクス演算
matrix operation
初期化
S301
initialization
注目画素アドレス抽出
(マトリクス演算すべき
注目画素を確認)
S303
extract address of target pixel
(confirm target pixel that is to be
subjected to matrix operation)
S305
エッジ
or 網点 ?
No
edge or halftone dot?
Yes
S307
No
入力メモリ
アクセスO.K ?
input memory can be accessed?
Yes
5*5画素マトリクスデータ
読み出し
S309
data read out of matrix
of 5 X 5 pixels
S311
網点 halftone dot
edge
エッジ
S321
smoothing
process
スムージング処理
エッジ強調処理
edge
enhancement process
γ処理
S313
γ correction
S315
No
出力メモリ
アクセスO.K ?
output memory can be accessed?
Yes
出力メモリへデータを書き
込む
S317
write data into output
memory
S319
No
全データ終了 ?
completed for all data?
Yes
エンド
end

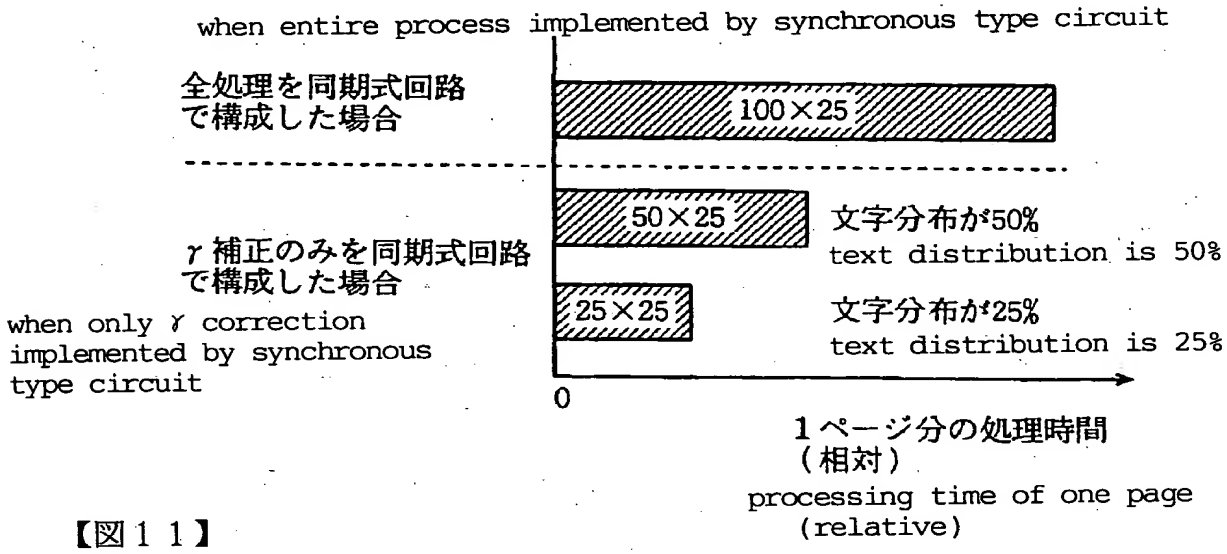
【図８】
Fig. 8


301
入力画像メモリ
input image memory
input data
入力データ
input memory control
303
入力メモリ制御
305
γ補正
γ correction
307
出力メモリ制御
output memory control
311
出力画像メモリ
output image memory
データバス
data bus
マトリクス演算
matrix operation
309
出力データ
output data

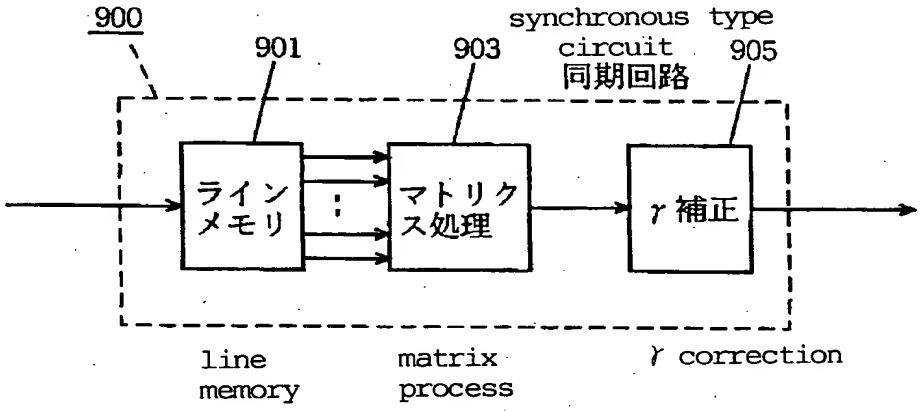
【図９】
Fig. 9


マトリクス演算
matrix operation
初期化
S401
initialization
処理対象となる注目画素アドレスを読み出す
S403
read out address of target pixel that becomes the subject of processing
入力メモリからデータを読み出す(M×N マトリクス分)
S409
read out data from input memory (MXN matrix)
M×N マトリクスの演算処理
S411
operation process of MXN matrix
γ補正
S413
correction
出力メモリ制御の書き込みアドレスを確認
S419
confirm write address of output memory control
出力メモリへデータを書き込む(オーバーライト)
S421
write data into output memory (overwrite)
S423
No
全データ終了 ？
Yes
completed for all data?
エンド
end

【図１０】
Fig. 10



【図１１】
Fig. 11



[Document Name] Abstract

[Abstract]

[Subject] To improve the processing speed in an apparatus that carries out a plurality of image processing on image data.

[Solving Means] Image processing that allows high speed processing such as γ correction is carried out by a synchronous type circuit on all the region in document image data 100. Image processing is carried out by an asynchronous type circuit such as an MPU on a region that requires matrix operation such as the text region 100a, 100b in document image data 100. By synthesizing the processed results, one image data is obtained.

[Selected Drawing] Fig. 1